ART OF TECHNOLOGY

NEWSLETTER

electronic system design

February 2007

This newsletter is brought to you courtesy of Art of Technology, a leading European specialist for customer specific electronic system design and development in hardware, software and electronic miniaturization.

Art of Technology will be exhibiting at **Medtec** in Stuttgart. Please visit us from February 26th to March 1st at our **booth 619** in **hall 4.0**
If you need a free guest ticket please do not hesitate to contact us at ticket@aotag.ch.

MEDTEC

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Content

Art of Technology AG

Art of Technology offers the whole spectrum of services for electronics design and development in hardware and software. We work together with our customers and support their team with exactly the processes they need, or take over a whole system as turn-key project.
Especially Art of Technology's expert know-how in medical technologies and sensors combined with High Density Packaging (HDP) technologies for a cost optimized system miniaturization of electronic systems is nearly unique. This allows us to realize innovative solutions together with our customers.
Art of Technology is ISO9001:2000 and ISO13485:2003 certified.

Please visit our new homepage on www.aotag.ch and learn about the services and support Art of Technology can offer you.

Yours sincerely
Rolf Schmid
Managing Director, Art of Technology AG

Technologies

High Density Packaging (HDP) vs. ASIC Design: Competing miniaturization technologies or synergetic partners?

from Dr. Thomas Gillen and Rolf Schmid, Art of Technology AG

Nowadays a steady obligation to product innovation exists: increased functionality, increased portability, volume and weight reduction, lowered power consumption. This obligation requires constant product improvement and increase of integration while simultaneously retaining or reducing unit cost. In order to reach the above goals the market offers, apart from the continuous improvement of the circuit principles, above all ASICs and HDP as integrated-circuit technologies.

ASIC designates the integration of different circuit parts (e.g. analog, digital, memory, optical components) on a chip with a fixed process (e.g. CMOS, CMOS/Flash, BiCMOS, etc.) and structure width (0.8µm, 0.35µm, …).

HDP covers all high-density interconnection and assembly techniques, which allow a miniaturization of an electronic circuit through the use of usually unpackaged ICs and high-density substrates. This technology is closely related to the standard SMD technology.

These two technologies shall now be judged regarding their basic criteria, type of circuit, complexity, and numbers of items and compared according to their parameter, cost, risk and turn-around time.

Type of circuit & complexity

Most suitable for integration are purely digital circuits. Here was the largest progress in the past, and following, analog circuits have been more and more digitized, in order to profit from this integration potential. In the consequence the gate numbers of purely digital ASICs raised more. Accordingly a wide range of tools (IP core,…) is available and supports all phases from the draft over prototyping up to the realization. But the progress of FPGAs and more efficient processors with flexible periphery take over however more and more applications form the pure digital ASIC. Accordingly the offer of gate array with complexities up to some 100,000 gates sinks while at the same time NRE costs and minimum order quantities rise.

The advantage of a pure digital ASIC integration is the size reduction, the encapsulation of the circuit complexity and the lower unit prize compared to off the shelf components at a relatively low integration risk.

Already when integrating non-volatile memory care must be taken: a mixed CMOS/Flash process lies in its production costs about 30% higher than a pure CMOS process. Here HDP offers the possibility through skillful partitioning of the system to spread the integration load and to optimize the costs, through the use of dedicated chips (memory, processor) for standard functions and to realize only the remaining parts in a customer specific ASIC.

Purely analog circuits are likewise well suited for an ASIC integration, since they can often be implemented only by a big number of discrete units; they require however a very good specification of the system part that has to be integrated.

In the contrary, mixed signal applications are complex in the design and in the process realization: Logic components must be e.g. transferred either into a BiCMOS process or analog elements have to be ported to CMOS. Due to the contrary requirements often important system features have to be sacrificed, which leads in the long run to the discontent with the result. The risk rises exponentially if the desire for the integration of e.g. optical components or flash memory arises.

From ASIC developers, this risk is often seen as challenge; the management however is often not informed about possible risks and useful backup strategies. Sorrowful experiences especially in SME with mixed signal systems are well known and often an ambitious project had to be stopped or terminated with a very low process yield.

In mixed signal systems HDP offers the advantage to combine standard components and ASICs, whereby each part can be realized in the optimal technology process. The packaging is then made on the module or system, whereas the result does not have to be compellingly larger or more expensive than the desired one chip solution!

Production volumes

An ASIC development always means a considerable expenditure regarding development time and work, NRE, prototype turnaround time and cost. In addition the component must be packaged and qualified. A certain minimum volume is thus necessary, over the 3M thumb rule (1Mio gates, 1Mio units, or 1Mio $) one may argue.

The wages of these troubles exist in the later reduction of the unit cost by „the Economics of Scale" and the fact that only the parts that are really needed are integrated. However the expenditure must always be amortized over the projected number of production volumes, any changes of process and migrations come down at least to a new qualification, possibly to a redesign.

When talking about the NRE one must plan at least slight below 100'000 EUR for a silicon run including masks for one semi custom mixed signal ASIC, for more complex digital designs quickly several 100'000 EUR are needed – for each needed production run (e.g. for the removal of errors)! The Design costs are not yet considered thereby; lie however at least in the same range.

Regarding NRE and prototype cost MPW runs offers a good alternative for cost reduction. However to the price of the flexibility (certain processes are only run once per year, fixed dates, etc.). Afterwards still the transfer to a volume manufacturer must be made. With lots of up to 20 wafer on 6-8" lines and small ICs very quickly some 10'000 pieces or more are produced per lot, which possibly correspond to the need for several years, reduces flexibility and blocks a lot of capital. On the other hand side it's a protection from discontinued components anouncements.

Design phases last from several months to years (with most complex designs), prototype run need 2-4 months, not included packaging and test.

Through the increased use of CPLDs and FPGAs, for purely digital designs the minimal quantities have been raised more than for mixed mode designs. The use of pre-structured ASICs, also within the analog range (analog gate array) allow an economical realization even for smaller volumes, however with reduced flexibility.

HDP is suitable in principle from smallest to middle quantities. When using largest volumes a combination with ASICs is used (e.g. chip on board in clocks or toys from the Far East). The needed bare dies are often available either as samples or in small volumes of some 100 pieces (corresponds to one wafer). Suppliers are often skeptic at the beginning, but depending on the product they can be convinced to supply for volumes of only a few 10'000 pieces/a, volumes, which are uninteresting for most ASIC manufacturers.

The HDP development times depend on the component availability and are in the range of 4 - 6 months (inclusive prototype supply). Development costs for the transfer of a design to a HDP solution depend upon complexity but are between 25'000 EUR and 50'000 EUR. Prototypes normally cost 10-20'000 EUR.

	ASIC	HDP Technologies
System size	smallest	Very small
Cost per piece	Smallest (for running process with high yield)	Small
Initial development cost	High to very high (some 100k to over 1 Million EUR)	Moderate (few 10k to 100k EUR)
Needed annual volume	>> 100'000 units	From 100 units on
Design risk	Often very high, especially for mixed signal	Relatively low
Prototypes available (from project start)	~ 12-24 Month	~ 4-6 Month
Typical application areas	Consumer electronics, Mobile phones, Automotive,…	Medical, Industry, Sensors, Automotive, Aerospace …

Table 1: Comparison HDP-Technologies - ASIC Design

Summary

HDP and ASIC are two different integration technologies, each with its specific pro and cons, which are not mutually exclusive, but rather supplement. A HDP system can always later be realized as an ASIC, and an ASIC can also be used in a HDP Design, in order to make the next integration step!

However, in principle one can regard HDP as „the small “solution, with which fast results with fewer risks for smaller volumes are available. Through the complexity of the design and the tools ASICs are rather used for longer period strategies and high volumes, whereby the low unit cost prices and reduced assembly expenditure on board level are the driving forces.

The answer of the entrance question must be: HDP and ASIC are synergetic partners, which represent in an optimal combination suitable integration solutions for each type of circuit of high and low complexity and any volumes.

Application

GPS Logger for OEM Applications

The new GPS Data Logger is a complete system including antenna, battery and charger. It logs GPS data to a non-volatile memory, read out over USB. In addition to the Miniaturized GPS Logger presented in the last newsletter several additional interfaces increase the range of possible applications it can be used in. It has an increased sensitivity and extended runtime. The download software allows presenting the logged data in various formats.

Key features

- Size: 62 x 48 x 22 mm^3 (in a housing)
  58 x 43 x 8 mm^3 (only print without battery holder)
- Weight: 65 grams in housing
- Runtime ranges from 18 hrs “continuous” (2.5Hz) sampling, with primary cells, up to several days in adaptive modes
- Up to 320’000 position fixes with time stamp. Equivalent to four month with one fix per 15 seconds logging 11 hours per day.
- Flexible configuration
- 16 channel low power LEA-4A GPS receiver module from u-blox AG (see www.u-blox.com)
- 2x AAA Li-Ion rechargeable batteries or 2x AAA primary cells
- Internal battery charger
- ATmega128L processor
- 32Mbit data flash
- 3 Buttons
- Optional display
- On board (not connected to the housing)
  - 4 digital inputs of which 3 can be used as analog inputs
  - 4 digital outputs
  - Power- or battery input 1.6 – 4.4V
  - External antenna (passive or active)

Purpose
The logger has been developed as a base for OEM applications where storage of GPS data and additional signals is needed. The GPS logger can be extended to various different systems. In combination with communication (RF, Bluetooth, ZigBee, GSM), further sensors (movement, temperature, humidity) and/or intelligent software the device can be used not only for logging and communication data but also to trigger alarms.

Possible application areas could be:

- Tracking of security patrol
- Surveillance of animal behavior
- Environmental surveillance

For further information visit us at Medtec 2006 in Stuttgart, February 27th – March 1st, 2007, Booth 619 in hall 4.0 or contact us at: info@aotag.ch

Industry News

Rigid-Flex Prints

Meta Leiterplatten GmbH & Co. KG offers single and double sided rigid-flex prints. In addition also multi-layer prints with up to 10 layers can be delivered as rigid-flex version. The minimal laser drilled via diameter is 0.10 mm. The recommended surface is chem. Ni/Ag. The company is producing according to IPC-A-600.

For further information see: www.meta-leiterplatten.de

Medical 400W power supply

Condors (distributed by Fortec) GNT400 series offers 400W output power in a 4”x7”x1.5” U-chassis. The series consists of four models with output voltage of 12V, 24V, 36V and 48V. When operating with convection cooling up to 300W power can be drawn. The power density of the device is 9.5W/inch^3. In the medical version the leakage current is below 100µA .

For further information see: www.fortecag.de

AC/DC converter for medical application

Schukat electronic offers the compact AC/DC modules of PM-series from Mean Well. Designed for print assembly, the modules correspond with the EN60601-1. Embedded in isolating plastic enclosures they offer isolation class II and have a low idle loss: up to 1W below 0.5W and from 20 W below 0.75W.

For further information see: www.schukat.com

Upcoming Events

Medtec 2007
(AoT will be exhibiting)
February 27th – March 1st 2007
Stuttgart, Germany
www.medtecshow.de

SMT/HYBRID/PACKAGING 2007
April 24th-26th 2007
Messago, Nürnberg, Germany
www.messago.de/smt

IFA 2007
August 31th - September 5th 2007
Messe Berlin, Germany
www.ifa-berlin.de

go 2007
September 4th-7th 2006
Messezentrum Basel, Switzerland
www.go-automation.ch